The Facility for Antiproton and Ion Research is a new experimental structure that is under construction at the present GSI laboratory in Germany. It will host the PANDA experiment that is based on a fixed target apparatus, devoted to antiprotons physics study.

In the central region the Micro Vertex Detector (MVD) is placed for the detection of the position, the timing and the momentum of the incoming particles. The detector will be composed of a barrel with 4 coaxial cylinders, and a forward structure made of 6 forward disks [1]. The hybrid pixel sensor was chosen for the inner layers to achieve the required spatial resolution, while the double sided strip was selected for the outer layers to manage a large coverage.

The first layers of the pixel sensors are very close to the interaction point, for that reason the radiation tolerance has to be assessed both for the Total Ionizing Dose (TID) and the Single Event Upset (SEU). Considering an experiment lifetime of 10 year and a duty cycle of 50 %, a TID of 100 kGy is expected and a foreseen fluence of $10^{14}$ neutrons$\text{MeV equivalent}/\text{cm}^2$.

The readout circuit for the hybrid pixel sensor is a custom project called Topix, and it is made in a 130 nm technology [2]. The main section of the ASIC is the array of pixels, each one with a size of 100 $\times$ 100 $\mu$m$^2$ and containing both the analogue and digital parts. The analogue chain features an input dynamic range up to 50 fC, and foresees a Charge Sensitive Amplifier with capacitive feedback. It also includes a comparator to discriminate the amplifier output for the Time Over Threshold (TOT) determination, with a level that can be adjusted on a channel by channel basis.

At present, the current solution to transfer the event information outward the MVD is the GigaBit Transceiver (GBT) developed at CERN. The GBT is a large project for the data transmission on optical links, envisaged for the next generation experiments that will work with high luminosity beams [3]. The purpose of the system is to provide a bidirectional serial link at high speed, featuring a high radiation hardness. The whole project consists of several ASICs to implement the link on the detector side, followed by electronics placed in counting room that are some memory elements to store the timestamp values of the comparator leading and trailing edges, from which the TOT is extracted. These registers are both 12 bit long, then there is an 8 bit long register with configuration parameters as the local fine threshold or the testing pulse enable. Due to the low available space all the registers are implemented with latches, and they are protected against the SEU by the Triple Modular Redundancy (TMR). The device under test is reduced scale prototype with 640 cell distributed on 4 columns, instead of the 12760 cell foreseen for the final circuit [4].

The pixel matrix of the Topix circuit is organised in columns with a specific bus that conducts the data toward the edge of the circuit, where they are stored before the serialization. The memory element is based on a FIFO structure that is composed of a 32 word array, where each entry is 40 bit long. The stored information regard the time stamps of the leading and trailing edges, followed by the cell address of the hit pixel. In this end of column region the SEU protection is implemented with the Hamming encoding that, adding some extra bits, is able to detect and correct one bit error.

The GBLD circuit make use of the same 130 nm technology used for Topix, and it is designed to work at 4.8 Gbit/s but it is running well up to 10 Gbit/s. The laser driver is able to control both the VCSEL and the EEL laser diodes, and a pre emphasis is available to manage a load with high capacitance [5]. The bias current and the modulation current can be adjusted by means of a serial FC interface, integrated on the GBLD. The actual configuration is saved in 7 register with 8 bit that are physically implemented by D type flip flops, and the SEU protection is obtained with the TMR as in the Topix cell registers. To address some user requirements, a new version called Low Power GBLD (LPGBLD) was designed to control VCSEL diode only. Besides the difference on the circuit, the GBLD uses a layout with thick metal layers for large currents while the LPGBLD employs the standard layers.
THE MEASUREMENT AND THE RESULTS

The SEU measurements were performed at the Sirad facility, where several ions are available to test the samples positioned in a vacuum chamber. The Sirad facility provides also a system to evaluate the actual dosimetry, by monitoring the instantaneous flux and the integrated fluence of the ions with silicon diodes. The measurements were executed with a large range of ions energy, from Oxygen (O) at 101 MeV up to Chlorine (Cl) at 197 MeV. The devices under test are set in a working state and their configuration are checked every 2 s: when a change is observed the error counter is incremented and the circuits are configured again to the default states.

The ratio between the registered errors and the incident ions allows the estimation of the upset frequency, that has to be normalised with respect to the number of bit in the Topix prototype. At present that number corresponds to the configuration register length times the pixel cell quantity, that returns 5120 bit. The obtained cross sections are represented as a function of the Linear Energy Transfer (LET) of the respective ion, and fitted as usual with a Weibull function. For the configuration register of the Topix sample, a saturated cross section of about $2 \times 10^{-8}$ cm$^2$/bit is resulting. Besides such configuration register, protected with TMR, shows its threshold to the upset for a LET greater than 2 MeV cm$^2$/mg.

Regarding the FIFO structure for the Topix circuit the number to use for the normalization is the word length times the FIFO depth times the column number that means again 5120 bit. The measurement of the saturated cross section is around $7 \times 10^{-9}$ cm$^2$/bit and the LET threshold is about 1 MeV cm$^2$/mg, for the structure that is protected via the Hamming encoding. The comparison with the Topix configuration register points out that the TMR protection is more effective that Hamming code, with respect to both the cross section and the SEU threshold.

For the standard GBT, designed to drive both the VCSEL and the EEL diodes, the number to use for the cross section normalization is the register length times the register number that returns 56 bit. The layout, that includes D type flip flops and features thick metal layers, is the same foreseen for the final ASIC. The measurement of the cross section, for that structure protected with the TMR, shows a value around $4 \times 10^{-9}$ cm$^2$/bit (figure 1). For what is regarding the threshold of the effect, the result of the test is about 2 MeV cm$^2$/mg.

The LPGBLD, designed for low current consumption with standard metal layers to drive VCSEL diodes only, has the same logical interface of the previous circuit and therefore the normalization number is again 56 bit.

Also in this case the register array was protected with the TMR, and the test result shows a saturated cross section of roughly $3 \times 10^{-9}$ cm$^2$/bit. Measuring the threshold for the appearance of the upsets, again a value around 2 MeV cm$^2$/mg is obtained. So the two laser driver samples, even though they come from different requirements and designs, have implemented the same protection method and that implies a similar saturated cross section.

![GBLD v4](image)

**Fig. 1. Cross section for GBLD registers with D type flip flops.**

The saturated cross section for the Topix configuration register is an order of magnitude larger than one for the GBLD circuit, and that is probably due to the latches used in place of standard flip flops. Tacking advantage of the experience acquired on the GBLD test, the new Topix version will use the D type flip flops.