Using Ion Electron Emission Microscopy to Study Current Spikes in NAND Flash Memories

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INTRODUCTION

Today Flash memories are attractive for space applications, due to their non-volatility, large capacity, low cost, and small power consumption [1]. Ionizing radiation effects should be carefully addressed before using them in space [1]. Although a huge amount of work has been performed in the past, there are still open issues concerning single events and total dose response of these devices. Single event effects are becoming more and more widespread and complex, due to charge reduction in the floating gate and the increasing complexity of the control circuitry. Anomalous spikes in the supply current during heavy-ion exposure and seemingly correlated destructive events have been recently observed [2,3].

In this work, we investigate supply current spikes using first heavy-ion beams and then the ion electron emission microscopy technique [4]. By correlating the spike events with the ion impact locations, reconstructed with micrometer accuracy, this technique allows us to pinpoint positional information on the device response.

DEVICES AND EXPERIMENTAL DETAILS

We studied 90-nm multi-level cell NAND Flash memories fabricated by Samsung (K98GG08UOMPCB0). The memories were irradiated with heavy ions, using a broad beam at the SIRAD irradiation facility of Legnaro National Laboratories [5]. If a current spike was detected, the beam was immediately stopped and power was cut to the device. Before resuming the irradiation, functionality tests were performed on the Device Under Test (DUT).

In addition to broad-beam experiments, an Ion Electron Emission Microscope (IEEM) was used. The IEEM [4] is devised to provide a micrometric sensitivity map of SEE of an electronic device. The IEEM reconstructs the positions of individual random ion impacts over a circular area of 180 µm diameter by imaging the ion-induced secondary electrons emitted from the target surface. A 100-nm thick Si₃N₄ window with a 30-nm Au deposition is mounted on a frame in front of the DUT. A photo-electron emission microscope focuses the impact generated secondary electrons onto a micro channel plate coupled with a phosphor screen. The image is then delivered to a custom-made fast data acquisition system that reconstructs the spatial and temporal information of each ion impact. Any signal induced by SEE in a generic DUT can be used to tag the IEEM reconstructed event. This information is then used to display a map of the regions of the DUT which are sensitive to the heavy ions [4]. In this work, spikes in the current of Flash memories were used to tag IEEM events.

RESULTS AND DISCUSSION

Fig. 1 shows the results of broad-beam irradiation (266-MeV Ag) on a NAND Flash memory in idle state during exposure. Current spikes were continuously detected. The status of chip select, a signal that determines if the memory is in standby or ready to operate, does not impact the occurrence and frequency of the current spikes. When the chip is unselected, several functional blocks are turned off, in order to save power. These circuits possibly include the decoders and the microcontroller, which, therefore, should not be involved in this phenomenon. In addition, if the control circuitry area is shielded, no spikes occur.

![Fig. 1. Supply current at 266 MeV Ag (LET= 56 MeV /mg·cm²) broad-beam exposure. After each spike the beam was stopped and power was cut to the chip.](image)

We observed that the supply current goes back spontaneously to the normal level, when the beam is stopped, ruling out single event latch-up as a possible interpretation. The cross section for all spikes obtained with broad-beam is 1.9·10⁻⁴ cm² (LET= 56 MeV /mg·cm²) and 2.7·10⁻⁶ cm² for spikes exceeding 10 mA.

Following these observations, we exposed a large part of
the chip area not occupied by the memory array to a collimated beam with a radius of 90 μm and, using the IEEM, we pinpointed the locations of the sensitive spots. Fig. 2 shows a sensitivity map of the memory obtained with the IEEM, overlaid to a picture of the die [6]. This map is the result of the combination of several different irradiation runs. Two regions were identified where supply current spikes occur, in the area of the peripheral circuitry. The cross section for spikes obtained with the IEEM at an LET of about 56 MeV·mg⁻¹·cm⁻² is about 1.2·10⁻⁴ cm⁻², slightly lower than the broad-beam measurement. This value has been calculated by measuring the area of the sensitive region displayed in Fig. 2.

Fig. 2. Sensitive areas for supply current spikes with 297-MeV I. Two distinct regions were identified with the IEEM. The picture of the die was taken from [6].

Our data indicate that there is no correlation between the amplitude of the current spikes and the irradiated area. In particular, Fig. 3 shows a portion of the sensitive area where high-current events (> 80 mA, red points) occur very close to low-current events (blue points).

Unfortunately, we do not have the exact memory layout, but we can draw some interesting conclusions. The fact that the current spikes tend to recover spontaneously seems to rule out the possibility that a single event effect in a control logic register triggers the sudden increase in current. Indeed, one should assume that the upset is then somehow corrected, which seems very unlikely. Of course, upsets in the microcontroller logic do occur, forcing the user to reset or power-cycle the memory to restore the functionality, but there is no evidence that these functional interrupts (observed for instance in [3]) are linked to the current spikes. Furthermore, we clearly identified two distinct areas, almost symmetrical with respect to the main axis of the chip, and it is unlikely that the embedded microcontroller is split into two parts.

Another interesting point is that, contrary to previous reports [2], our data indicate that the supply current spikes do not originate in the area of the charge pump capacitors, placed at both sides of the chip (see Fig. 2), far enough from the sensitive areas.

In addition to capacitors, other blocks are necessary to generate the high voltages required by program and erase, placed in the area designated in Fig. 2 as “peripheral circuitry”. A reference voltage is produced and fed into the charge pump regulation circuitry. Oscillators provide the necessary clock signals (typically, two non-overlapping clocks are needed). Some control logic is then necessary to coordinate all the blocks. Several studies have been performed on the response of voltage regulators to single event effects [7]. In particular, single event transients could cause temporary variations in the reference voltage. Single event transients could also cause non-overlapping clocks to become overlapping. In both cases anomalous, but transient, supply current spikes could occur.

CONCLUSIONS

We investigated supply current spikes in NAND Flash memories, using both broad beam irradiations and the ion electron emission microscopy technique. Our experimental data suggest that the current spikes observed in these samples are due to single event transients in the analog support circuitry.