Alpha-induced soft errors accumulation and mitigation techniques
in commercial SRAM-based FPGAs

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INTRODUCTION

SRAM-based Field Programmable Gate Arrays (FPGAs) are an attractive solution for many applications where short time-to-market, low-cost for low-production volumes, and in-the-field-programming ability are important issues. One of the few major disadvantages of SRAM-based FPGAs is the sensitivity to ionizing radiation [1-3]. Indeed, also at sea level, neutrons, originating from the interactions of cosmic rays with the atmosphere, and alpha particles, coming from radioactive contaminants in the package and solder material, may alter the content of the configuration memory through Single Event Upsets (SEUs). A change in the configuration memory can modify the implemented circuit, possibly leading to Single Event Functional Interruptions (SEFI). Suitable hardening techniques are therefore needed to mitigate radiation effects in modern FPGAs. Hardening-by-design techniques such as Triple Module Redundancy (TMR) [4] are effective in preserving the design functionality when a SEU occurs. Experimental results are reported by first assessing the sensitivity of modern low-end SRAM-based FPGAs to alpha particles in both static and dynamic tests. Afterwards, we discuss the effectiveness of TMR techniques with different voting schemes in enhancing the system reliability, in the case where multiple errors are present in the configuration memory.

EXPERIMENTAL SETUP AND DEVICES

For our experiments, we used a Spartan-3 XC3S200 designed by Xilinx in a 90-nm CMOS technology. The device features 4320 equivalent logic cells, 12 dedicated multipliers, 4 digital clock managers, 170 user I/O, 30 Kbits of distributed RAM, and 216 Kbits of Block RAM.

Our test-setup comprises a Device Under Test (DUT) board and a control board. The control board can configure and readback the DUT via the Joint Test Action Group (JTAG) standard, stimulate the DUT and monitor the produced output. Radiation testing was performed at the Legnaro National Laboratories in air using an Americium source emitting alpha particles with an energy of about 5.4 MeV and flux of $1.5 \times 10^4$ alphas s$^{-1}$ within a solid angle of $2\pi$ sr. The half-time of $^{241}$Am is very long, 433 years, so the source can be modeled as a constant flux emitter. The distance between the FPGA and the alpha source was constant throughout our experiments. Prior to irradiation, the plastic package was etched through a nitric acid attack, leaving the die completely exposed.

TESTED CONFIGURATIONS AND CIRCUITS

Initially, we performed static tests to estimate the alpha-induced error rate of the DUT configuration memory controlling the various resources inside the FPGA. The DUT was loaded with ad-hoc configurations and the Americium source was placed above the exposed die. Periodically the control board scanned the configuration memory searching for bit-flips. Afterwards, dynamic tests were carried out, comparing the DUT outputs with those coming from a golden unit not exposed to radiation. The corrupted bitstreams were post-processed using CILANTO [5], to trace the bit-flips in the configuration memory back to the controlled resources inside the FPGA.

One of the applications chosen for the dynamic tests was the PicoBlaze, a soft 8 bit microcontroller freely available from Xilinx [6]. After assessing the sensitivity of the unhardened circuit to alpha-particles, we applied different mitigation schemes based on TMR. In particular we adopted the following three solutions: 1) One-voter TMR, the design is replicated three times and a majority voter is placed at the circuit output performing a bit-by-bit voting; 2) Partitioned TMR, the unhardened design is divided into different partitions. Each partition is replicated three times and a majority voter is adopted on each partition’s output; 3) X-TMR, hardening is performed using a commercial tool provided by Xilinx [7]. Feedback voters are inserted to keep the state of the finite state machines (FSMs) synchronized across each replica of the circuit.

All the circuits were clocked at 10 MHz during our tests, thus minimizing errors due to Single Event Transients (SET).

EXPERIMENTAL RESULTS

STATIC TESTS

The data collected during the static tests are presented in Table I (details about the various FPGA resources may be found in [8]). As shown, Look Up Tables (LUTs) are the most sensitive resource to alpha particles. In addition, for all resources the probability of $0 \rightarrow 1$ and $1 \rightarrow 0$ upsets are different, possibly due to asymmetric physical layout
and/or asymmetric capacitive load. We present only normalized cross sections, since we do not have enough information on the top layers to precisely estimate the alpha flux in the sensitive regions.

**DYNAMIC TESTS**

Concerning the dynamic tests, Table II reports the experimental results. As our data show, TMR techniques are very effective in mitigating soft-errors when a single SEU occurs in the configuration memory. When just a few SEUs accumulate in the configuration memory some of the considered mitigation solutions may completely lose their effectiveness. For instance, the failure rate of the one-voter TMR version is worse than that of the plain one with 16 errors on average in the configuration memory. Partitioned TMR can offer increased robustness, depending on the number of partitions in the design and the circuit itself. Yet, for large error accumulation, the improvement may be only marginal. The feedback voters introduced by X-TMR can further improve the application reliability, effectively creating a large number of partitions in the design.

**CONCLUSION**

We presented an experimental study on the alpha-sensitivity of low-end SRAM-based FPGAs, focusing on the occurrence of multiple SEUs in the configuration memory. We measured the alpha-sensitivity of the configuration memory cells controlling the different resources an SRAM-based FPGA embeds. We performed dynamic tests of a complex circuit with and without hardening solutions based on TMR, measuring the rate of functional interrupts during exposure. The robustness of each design was discussed as a function of the voting scheme and the number of SEUs accumulated in the FPGA configuration memory.

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