I. INTRODUCTION

In these last years several works have been devoted to study the radiation effects in CMOS components with ultra-thin gate oxides. No appreciable trapped charge is measured in oxide thinner than 5-6nm. On the contrary, the main oxide degradation is the appearance of leakage current across the oxide immediately after exposure to ionizing radiation. Radiation Induced Leakage Current (RILC) [1], Radiation Soft Breakdown (RSB) [2], and Single Event Gate Rupture (SEGR) [3] represent the most important degradation phenomena affecting ultra-thin oxides. SEGR appears only when high oxide electric field is applied during irradiation, resulting in a catastrophic breakdown, which puts an end to the device lifetime. It seems only a minor concern for ultra-thin oxide, as the reduced operational gate voltage is too low to efficiently produce SEGR. Both RILC and RSB are generated even at zero bias and are characterized by a current increase, which is much smaller than in Hard Breakdown (HB) regime, being a real concern only for a limited number of application, such as DRAM or Non-Volatile memories, where data retention may be hampered.

When considering long term device reliability, radiation is not the only concern as gate oxides are subjected to high fields during normal circuit operations. Indeed the irradiated oxides underwent an accelerated wear-out in time much shorter and even at gate voltage much lower than in case of fresh (not irradiated) oxides [4]. The time to breakdown reduction was associated to the formation of physically damaged region corresponding to the ion hits.

II. EXPERIMENTAL AND DEVICES

The used devices were square MOS capacitors grown on p-Si with oxide thickness $t_{ox}=3$ nm and gate area ranging from $10^6$ cm$^2$ to $10^7$ cm$^2$. The gate active area of MOS capacitors was surrounded by a n$^+$ doped ring, in order to supply electrons to the channel when a positive bias is applied to the gate. In our experiments we used 256 MeV I ions with LET=64 MeV-cm$^2$-mg$^{-1}$. Devices were irradiated by using the SIRAD irradiation facility of the Tandem Accelerator at the Laboratori Nazionali di Legnaro, INFN and Università di Padova, Italy. Device terminals were kept floating during irradiation, which is not the worst case condition for RSB as previously demonstrated.

We irradiated 120 capacitors at fluences from $10^6$ cm$^2$ to $10^7$ cm$^2$ I ions/cm$^2$. We measured the gate current vs. the gate voltage (IgVg) before and after each irradiation step. Both fresh and irradiated devices were submitted to an accelerated Constant Voltage Stress (CVS) at different gate voltages, namely $V_{CVS}=3.8$ V, 4 V, and 4.2 V, corresponding to an oxide electrical field $E_{ox}=9.7$ MV/cm, 10.2 MV/cm, or 10.7 MV/cm, respectively.

III. RESULTS

The effect of heavy ion irradiation on the wear-out of the gate oxide is shown in fig.1, where we present the excess gate current density ($I_e$) vs. time for three devices with same gate area ($10^{-3}$ cm$^2$) and subjected to different fluence values, showing a gradual degradation of the leakage current and an oxide lifetime reduction depending on the number of ions hitting the gate.

![FIG. 1: Gate current measured during CVS at $V_{CVS}=4.2$ V on 3 samples with gate area $10^{-3}$ cm$^2$ irradiated with 256 MeV I ions at different fluences.]

In fig.2 the ratio $I_e$/number of hitting ions vs time is shown suggesting the idea of a degradation proportional to...
the number of ions hitting the gate surface. In fig.3 we present the effect of irradiation on two samples with different gate area ($10^{-4}$ cm$^2$ and $10^{-3}$ cm$^2$) hit by the same number of ions. The devices show similar gate excess current likely due to the same number of RSB spots opened by electrical stress.

![Figure 3](image_url)

**FIG. 3**: Gate current measured in four samples, two irradiated and two unirradiated, during CVS at $V_{CVS}=4$ V. The two irradiated samples received different fluences but which were hit by the same number of ions ($~$1000 I ions).

**IV. PHYSICAL MODEL AND SIMULATIONS**

In order to simulate the accelerate wear-out of ultrathin oxides we started from the following hypotheses:

1. Irradiation produces a number of physically damaged regions $N(f)$, which depends on the radiation fluence $f$. Such regions is a precursor site for a subsequent breakdown (BD) event. Hence, at most $N$ BD events can occur during the electrical stress.

2. The time $\tau$ needed for each precursor to underwent BD is a random variable with exponential distribution:

$$f_{\tau}(t) = \lambda \cdot \exp(-\lambda \cdot t)$$  \hspace{1cm} (1)

where $1/\lambda$ is the average time a precursor need to underwent BD.

3. The precursor regions are independent each other. Therefore, the N precursors can be statistically described by a random variable each of them having distribution like Eq.1 with the same $\lambda$.

4. Anytime a BD event occurs the gate current increases of $\Delta I$. The value of the gate current increase has been estimated from the experimental curves. It assumes values in the range 50$\mu$A and 100$\mu$A wit a roughly uniform distribution.

For sake of simplicity we considered in the following a constant $\Delta I=70\mu$A, i.e., the average value dependence on time is:

$$<I(t)> = \Delta I \cdot N \cdot [1 - \exp(-\lambda \cdot t)]$$

**V. CONCLUSIONS**

We investigated the premature gate oxide wear-out occurring under electrical stress after heavy ion irradiation and we have proposed an innovative model based on a non homogeneous Poisson process. We modeled the progressive degradation of the gate current as the superposition of many SB events, whose occurrence times have been randomly generated with exponential distribution probability.

**REFERENCES**